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GENERAL DESIGN CHARACTERISTICS OF THE APOLLO GUIDANCE COMPUTER (C XX)

by

Eldon C. Hall

May 1963

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R-410

GENERAL DESIGN CHARACTERISTICS OF THE APOLLO GUIDANCE COMPUTER

ABSTRACT

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This report describes the Apollo Guidance Computer in its general design characteristics, flexibility, reliability, and in-flight repair capabilities. Since the Command Module computer and LEM computer differ basically only in form factor and therefore weight and volume, the characteristics detailed here apply to both types of computer. Conf. Author

by Eldon C. Hall

May 1963

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SECTION I
COMPUTER CHARACTERISTICS

The Command Module (C/M) computer and the LEM computer are electrically the same with interchangeable pluggable subassemblies. The form factors of the two computers are different, therefore the volume and weight of the two are different. The C/M computer is just under 2 cubic feet (see Fig. 1) (2 cubic feet is the space in the C/M allocated for the computer) and weighs approximately 110 lbs. This volume and weight contains the mechanical structure to support and interconnect the electronic modules, transfer the heat to the cold plate interface of the spacecraft, provide the electrical wiring channels for the G & N spacecraft interface, and last, provide storage space for spare parts since the computer does not use all the allocated space. The LEM computer (Fig. 2) is contained in a volume of approximately 0.9 cubic feet and weighs approximately 50 lbs. Figure 3 is a picture of the C/M computer using the LEM packaging form factors. The volume of this design is 1.5 cubic feet and it would weigh around 70 lbs. There is space within the volume allocated to add a complete tray of spare parts for the computer. See Appendix I.

As has been stated, both of these computers are electrically the same and include all interfaces with the presently understood LEM and C/M systems. Therefore, the following discussion of the functional capabilities of the computer applies to both of these computers. The C/M computer is required to operate two display panels, one associated with the G & N system at the navigational bay, the other associated with the spacecraft's main display panel. This computer has 24,576 words of fixed memory. Present thinking on the LEM computer is that there will be only one computer display panel and the memory capacity will be 12,288 words of fixed memory. A brief description of the computer characteristics are contained in Table I.

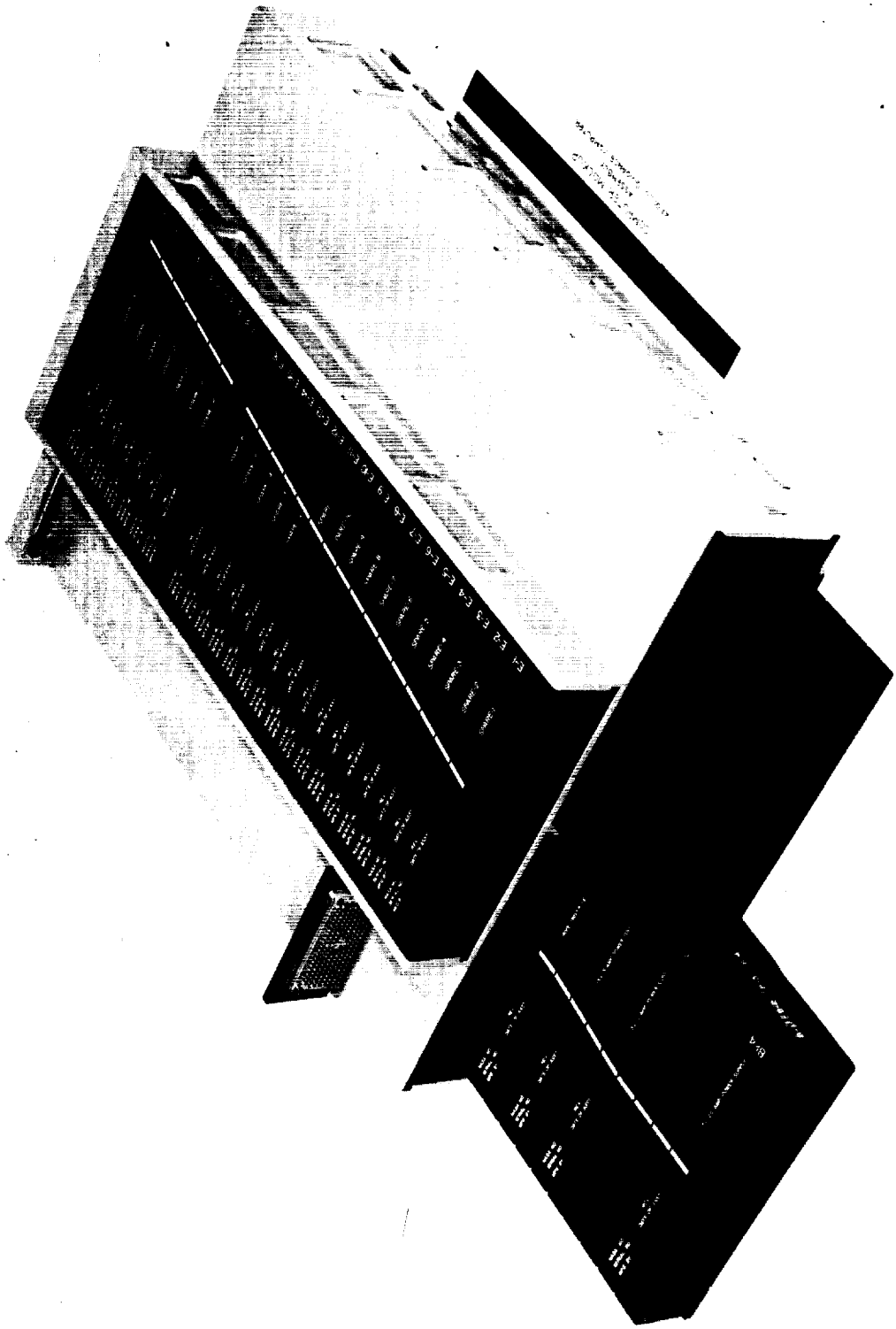


Fig. 1 Command Module Computer

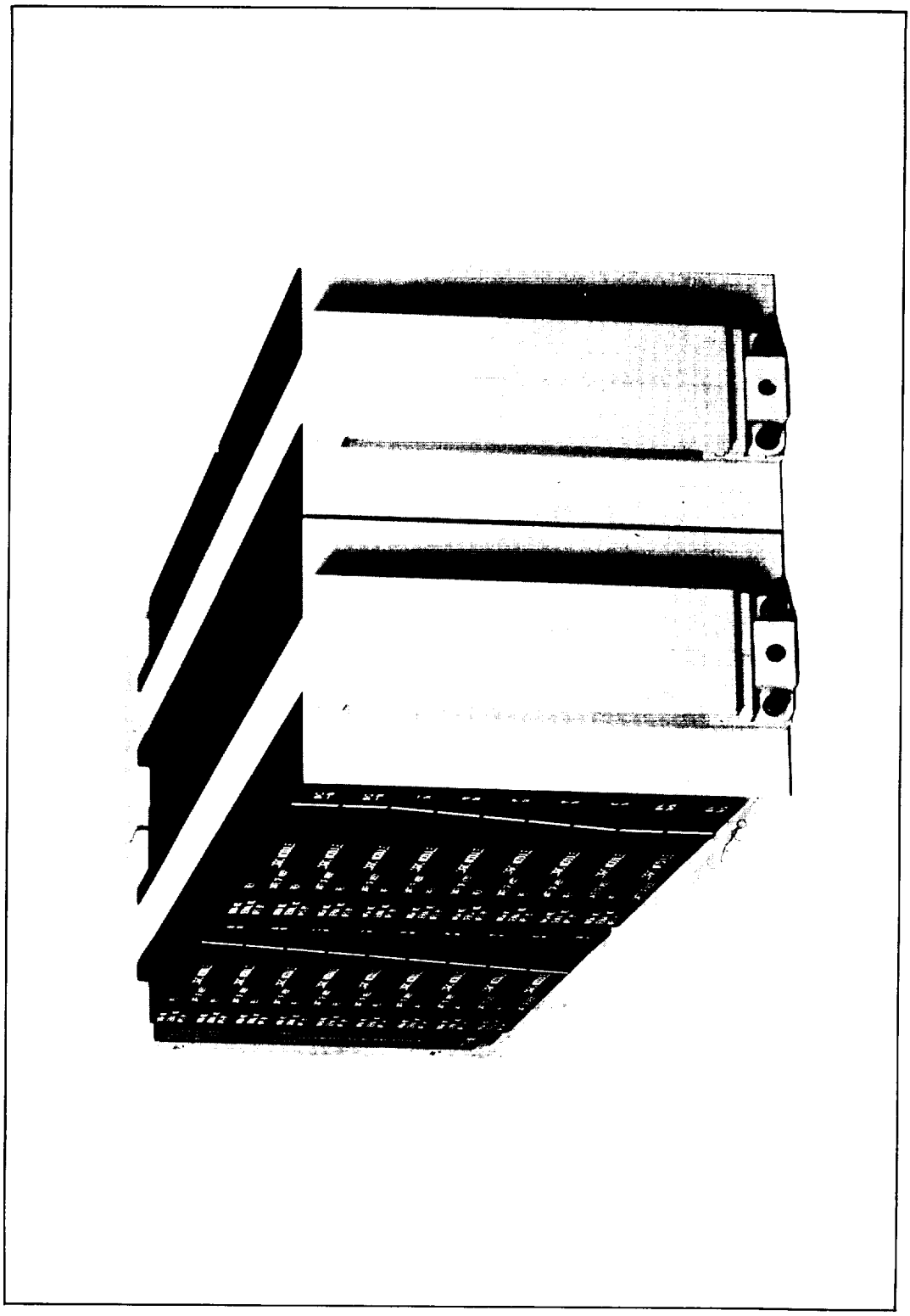


Fig. 2 LEM Computer

Power	100 watts (idle mode 10 watts)
Word Length: 16 bits (15 bits + parity)	
Number System: one's complement, with overflow correction	
Memory Cycle Time (MCT)	11.7 μsec
Wired-in memory (Core Rope)	24,576 words C/M configuration
	12,258 words LEM configuration
Erasable memory (Coincident current Ferrite)	1024 words
Normal order code	11 instructions
Involuntary instructions (Interrupt, Increment, Load, Start)	8 instructions
Interrupt options	5 options
Add instruction time	23 μsec
Multiply (excluding Index)	93.6 μsec
Double precision Add subroutine (X+x) + (Y + y) = (Z + z)	234 μsec
Double precision multiply subroutine	971.1 μsec
Counter incrementing	11.7 μsec
Number of counters (input)	20 counters
Discrete input registers	4
Discrete outputs registers	5
Pulsed outputs under program control	25
Pulsed outputs not under program control (Timing signals for S/C and G & N)	16
Telemetry: Signal processing for both up telemetry (or PACE digital command system) and down telemetry.	

Table I AGC Characteristics

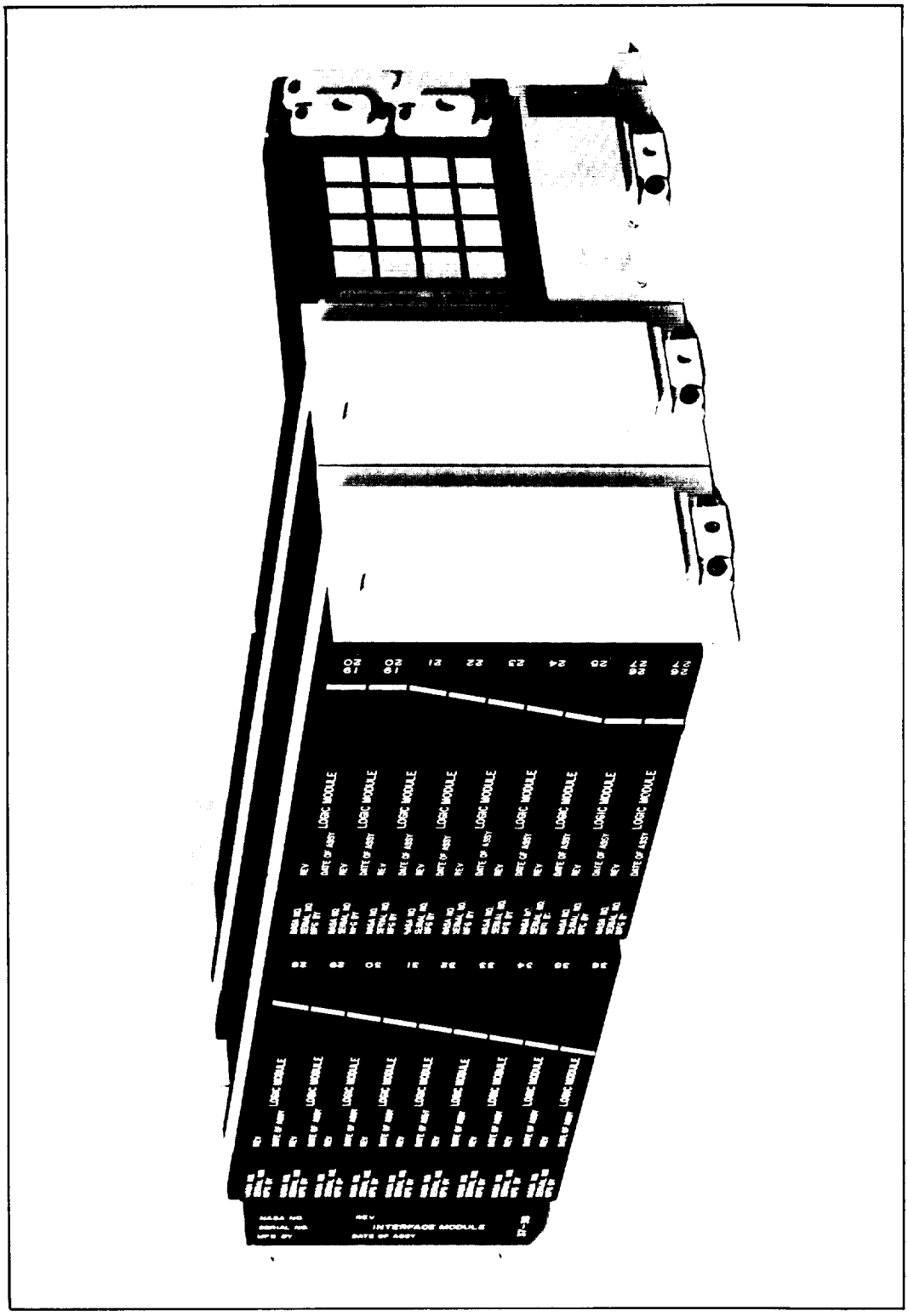


Fig. 3 New Command Module Computer

To further define the memory capacity and speed, we must look in detail at the characteristics of the machine. Appendix II, which was extracted from R-408, contains a description of these characteristics.

The AGC uses three types of memory circuits; one is for a permanent storage of instructions and constants and holds about 24,000 words. The second type is for the temporary storage of intermediate results, modified instructions, and input data. It holds about a 1024 words. Both of these types of memory are relatively economical and dense in terms of the number of words per unit volume. But they also require a comparatively long time to read from and write into (about 12 μsec). The third type of memory, consisting of 16 registers, has a read-write time of about 2 μsec and is about a 1000 times larger in volume than the other two types of memory. This group contains input and output registers which communicate between the computer and the rest of the Apollo system. The central registers participate in the instructions and cause the desired mathematical transformations to be effected. These three types of memory are employed to optimize requirements for reliability and flight maintenance without sacrificing the flexibility requirements of the guidance computer. The permanent memory requires very few active components and very little power to operate; it also has properties that make it indestructible short of mechanical dam age, that is, there is no inflight failure that can destroy this part of the memory. The temporary or erasable memory is a coincident current type similar to those used in most computers made in recent years. The cores are ceramic instead of metal but display the same characteristics, that is, high output, very low temperature sensitivity, and low drive power requirements. The central registers and the input-output registers are made using semiconductor networks (micrologic NOR gates). These gates are the same as those used throughout the computer for decoding operation codes and addresses, generating control

signals, pulse forming networks and translating networks. All of these functions are referred to as logic circuits. The speed of the computer depends in part on the transition times of the various logic elements used and upon the memory cycle time required to read and write into the memory which is 11.7 μsec. Figure 4 is a picture of an erasable memory which contains 1024 words of storage. Figure 5 is a picture of a rope memory stick which contains 2048 words of storage, and Fig. 6 is a logic stick containing 120 micrologic elements.

To further elaborate on the speed capabilities of the machine, we should consider the numbers quoted in the table, that is, the add instruction time 23.4 μsec, multiply instruction time of 93.6 μsec, double precision add of 234 μsec, and double precision multiply of 971 μsec. These numbers apply when the machine is programmed in what is called basic machine language. To increase the capabilities of the machine from the programming point of view and to reduce the memory required for processing complicated computational functions, interpreter instructions have been employed in the AGC. There are 72 interpreter instructions presently available*. These are instructions such as vector operations of various types, double precision add, and double precision multiply. When the interpreter is used, these double precision add and double precision multiply instructions take a longer time than when done in basic machine language. That is, double precision add requires approximately 1440 μsec and double precision multiply requires about 2690 μsec. The interpreter's main advantage is that it conserves memory and makes the programming of complicated arithmetic operations much easier. Therefore, a trade off exists between speed and memory consumed. The programmer can program the machine in machine language and realize the speeds quoted in the table for the basic machine. When computational time is not important,

* MIT/IL AGC Memo #2, A List Processing Interpreter for AGC 4, Charles A. Muntz, 1/7/62

the programmer can use the interpreter language and realize the savings in memory at the cost of machine speed. Many of the control type functions that the computer is required to do, such as: operation of the displays, telemetry, data processing, and the G & N control, will be done in basic machine language. The counter incrementing and interrupt features also save time and storage capacity required for the computer to service the interface functions. In general, the interpreter instructions are designed for the navigational computations involved and normally do not require high speed computation. In conclusion, the AGC is a very fast machine when operating in basic machine language and a very powerful computational tool when programmed with the interpreter.

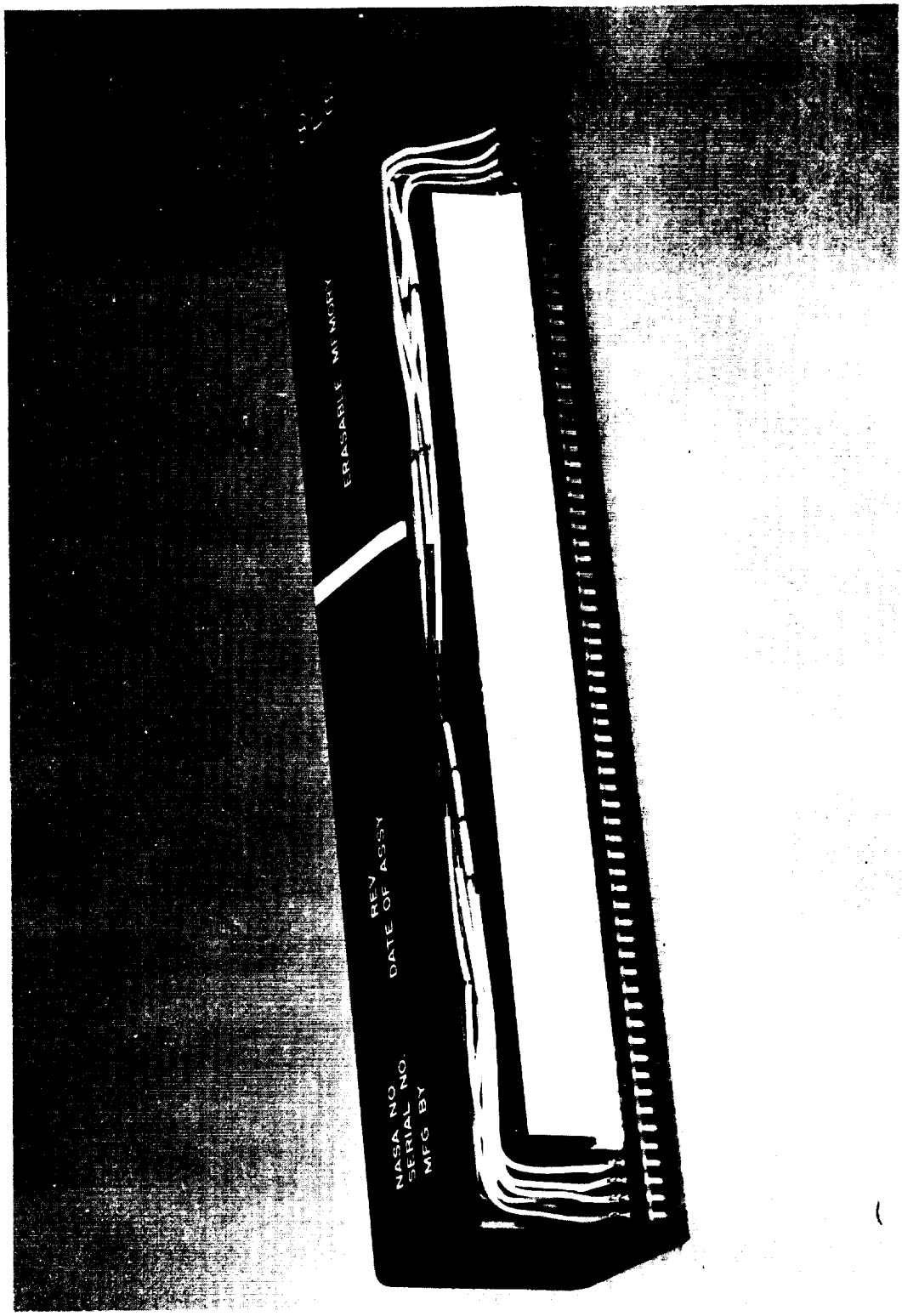


Fig. 4 An Erasable Memory Module

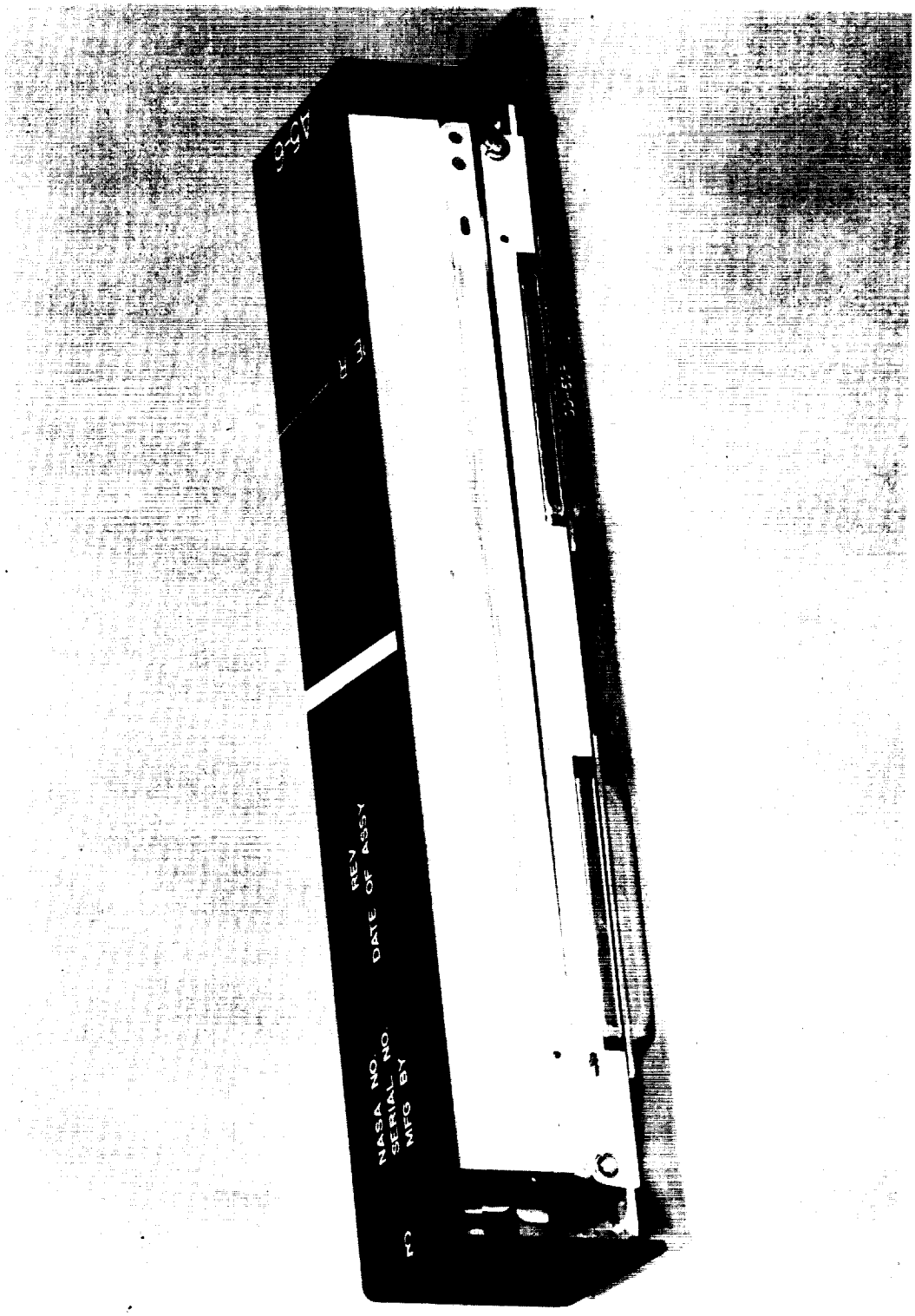


Fig. 5 The Fixed Memory Module

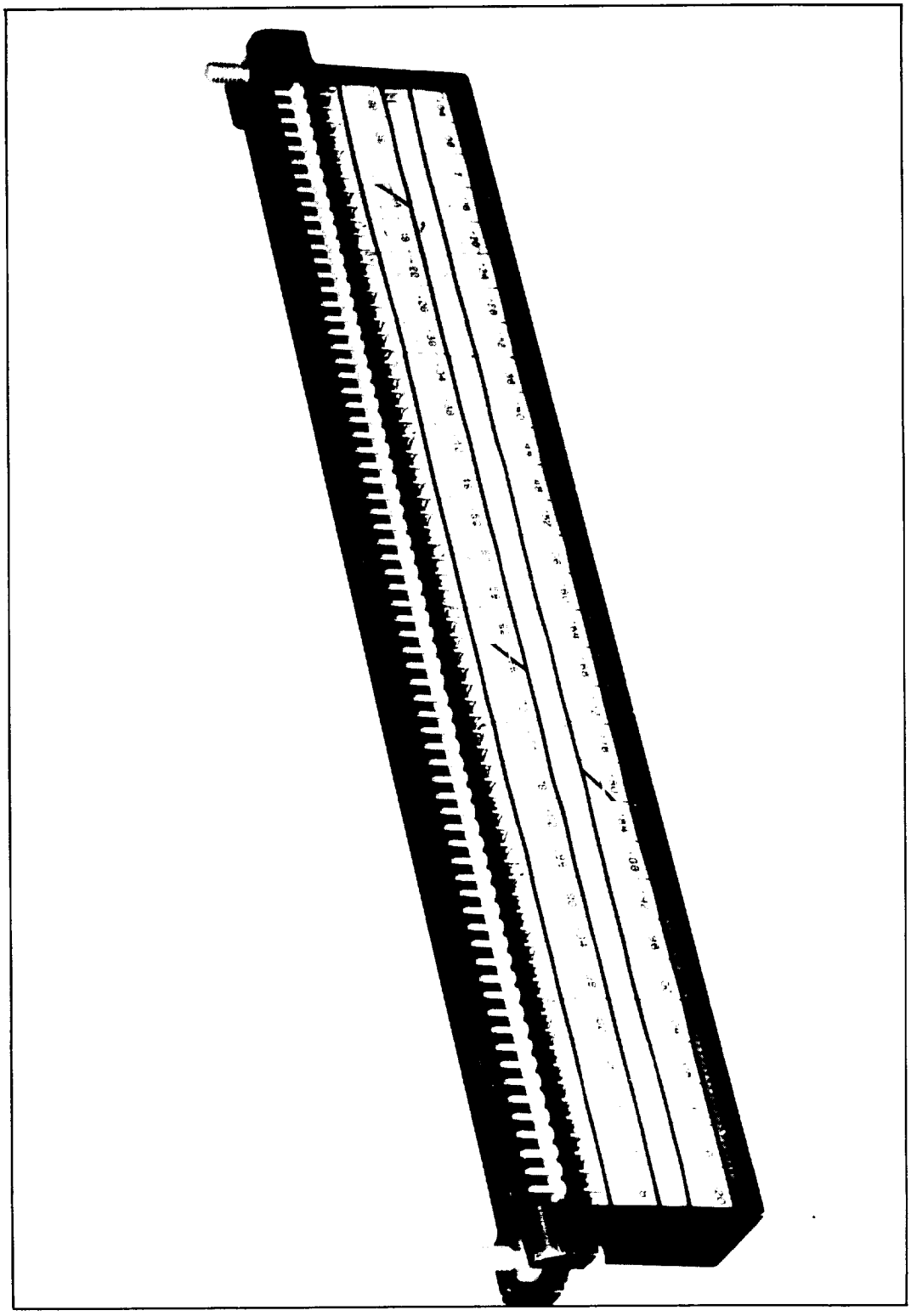


Fig. 6 The Logic Module

SECTION II
COMPUTER FLEXIBILITY

In the previous section the capabilities of the computer were described. From this description it is clear that the computer is a fast machine with a very large fixed memory for program storage. One might think that the fixed memory would make the machine somewhat less flexible than other machines with nondestruct type permanent storage. However with the techniques now available to build this memory in modular form (2048 words / module), the advantages of the fixed memory far outweigh any disadvantage that may arise in changing memory.

To explore the requirements of the system which will require changing the data stored in the computer memory, the following list is stated.

A. Changes due to Launch Window

The new data is updated by the digital command system of PACE every fifteen minutes during the countdown. Eight double precision words are required to be changed at these times. This data is read in automatically into the erasable memory. The data could be read in via the keyboard in the spacecraft.

B. Changes due to Astrodynamic Constants

Every two weeks these constants will have to be changed. To change these constants one plug-in fixed memory module will have to be changed. The data required for astrodynamic constants will be prepared well in advance of an anticipated flight, and memory modules built for each two week interval of anticipated launch.

C. Changes Required to Repair a Program "Goof"

It is this type of change which cannot be anticipated

and will require time to provide a new memory module. When considering the time required to produce a new memory (see Fig. 7) it is clear that the actual fabrication time is a small part of the overall problem of programming and verification of the program. The programming and verification cycle is independent of the type of memory used. Also, the module can be constructed during the time the program verification is being accomplished. The actual replacement of the bad module can be done in a few minutes at any point in the check-out sequence.

During system check-out a "goof" need not delay the check-out proceedures since the program changes can be made and read into the erasable memory for checking until the new fixed memory module is complete.

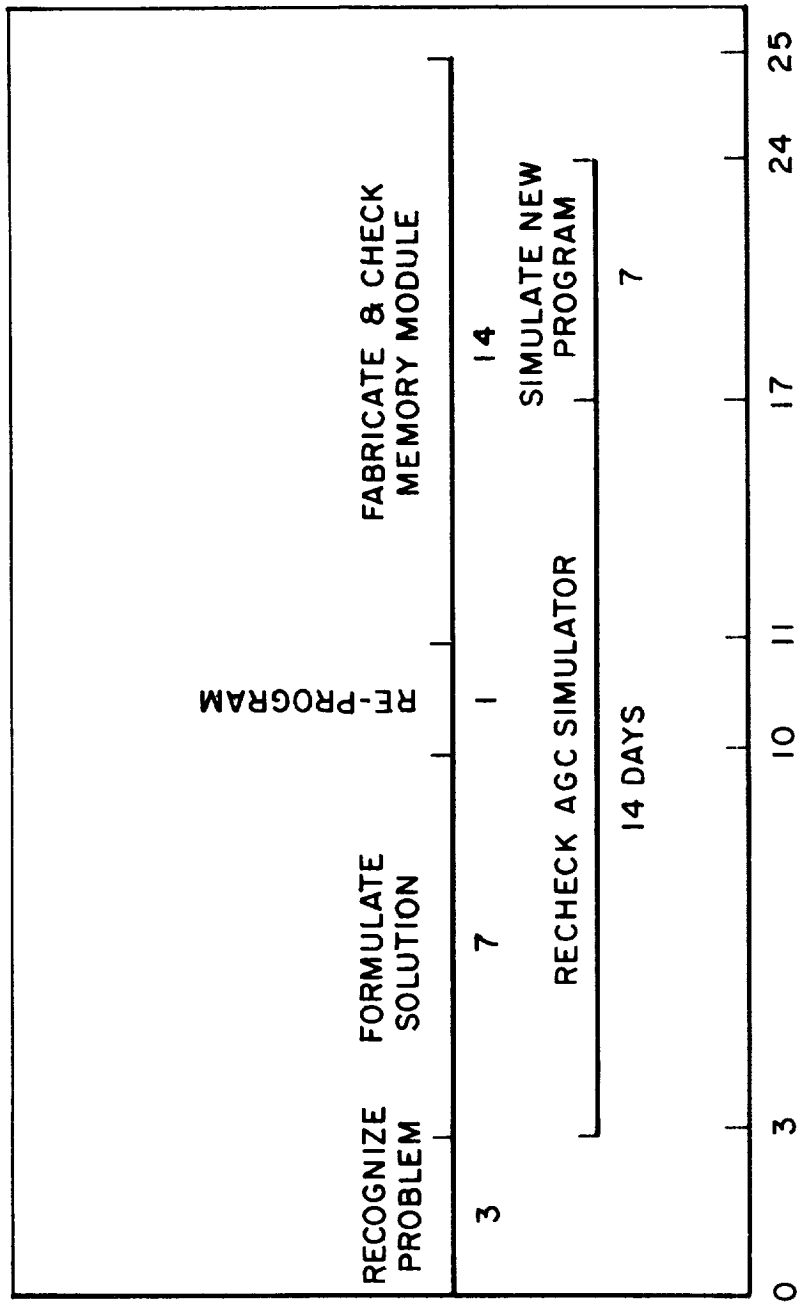


Fig. 7 Time Line Diagram

SECTION III
RELIABILITY

The MTBF that has been quoted in R-395 and in discussions concerning the reliability of the computer is one that is arrived at using present day figures on semiconductors and parts. Therefore, there is no projection into the future for increased component reliability. In addition, the computations in R-395 have assumed that failure in any single component in the computer will produce a failure of the computer. MIT has made reliability predictions on computers in the past using the same basic assumption and philosophy of reliability prediction. It has been demonstrated that these MTBF predictions are at least a factor of 4 lower than the MTBF realized in field operation. Also it is well established on computers using present day components that interconnections have been a greater cause for failure than components themselves. That is, the failure rates that are being realized on these computers in the field are due to failures of interconnections rather than failures of components. In mentioning failures due to connections, one should make the further comment that from the past history of these computers it is determined that the welded type connection is at least an order of magnitude more reliable than the solder type connections.

The computation of the MTBF in R-395 indicates the section of the computer with the highest failure rate is the logic section which contains the micrologic gate elements. This results from the large volume usage of micrologic and the component failure rate assumed. To reduce this predicted failure rate there is considerable work in analysis and specification of these logic elements; also tests are being run to determine failure modes and if possible to obtain a failure rate that has a higher confidence level than the one used.

From data published by the vendor micrologic failure rates are lower than 0.044%/1000 hours when operated in high stress conditions. By extrapolating this failure rate to the worst case computer operating conditions, the failure rate would be 0.01%/1000 hours[6]. The failure rate assumed in R-395 is 0.02%/1000 hours. It is therefore clear that the failure rate computed for the micrologic section of the computer is higher than should be expected. More data and tests are required to further verify these predictions.

When discussing reliability one should discuss the production techniques used to build a computer, since in many cases a large percentage of the failures can be attributed to the processes used in the assembly of the final computer from the basic components. The packaging and production techniques that are employed in the Apollo computer are identical to the techniques which have been used in production computers for several years at Raytheon where the Apollo computer is being produced. Therefore, the production techniques are well established, the bugs in these techniques have been worked out, and process controls have been improved and optimized for Apollo. This long production history will reduce the failures due to production problems to a minimum.

The MTBF quoted in R-395[4] assumes the computer is operating at full power 100% of the time. According to present planning of the mission profile, the computer is operated in idle mode for a large percentage of the time. Taking this fact into account, the MTBF for the complete mission becomes 4000 hours.

It has been suggested that the Apollo computer should be designed using redundancy to increase the MTBF. Redundancy is clearly undesirable from the point of view of volume, weight and power. It is not quite as clear what the trade offs are when considering inflight repair, however it is easy to say that if there is any inflight failure, and it is desirable to repair this failure, the repair of the redundant computer is more difficult. Another point

* Superscript numerals refer to the list of references at the end of this report.

should be made: triplicated, majority-type logic circuits* actually reduce the MTBF rather than increase it since there are more components involved in the redundant machine. To illustrate this, Fig. 8 shows the comparison. The redundant machine has a higher probability of success near zero time but the probability of success drops more rapidly and is lower than that of the nonredundant machine after an elapsed time equal to the MTBF of the nonredundant machine. To make redundancy pay, the nonredundant form of the machine should have an MTBF many orders of magnitude greater than the mission time. Also the start of the mission must be near zero time on the probability curve to make the probability of success very high. As a result an effective MTBF which is very high can be quoted.

* Wilcox, R. H. and Mann, W. C., Redundancy Techniques for Computing Systems, Spartan Books pp. 367.

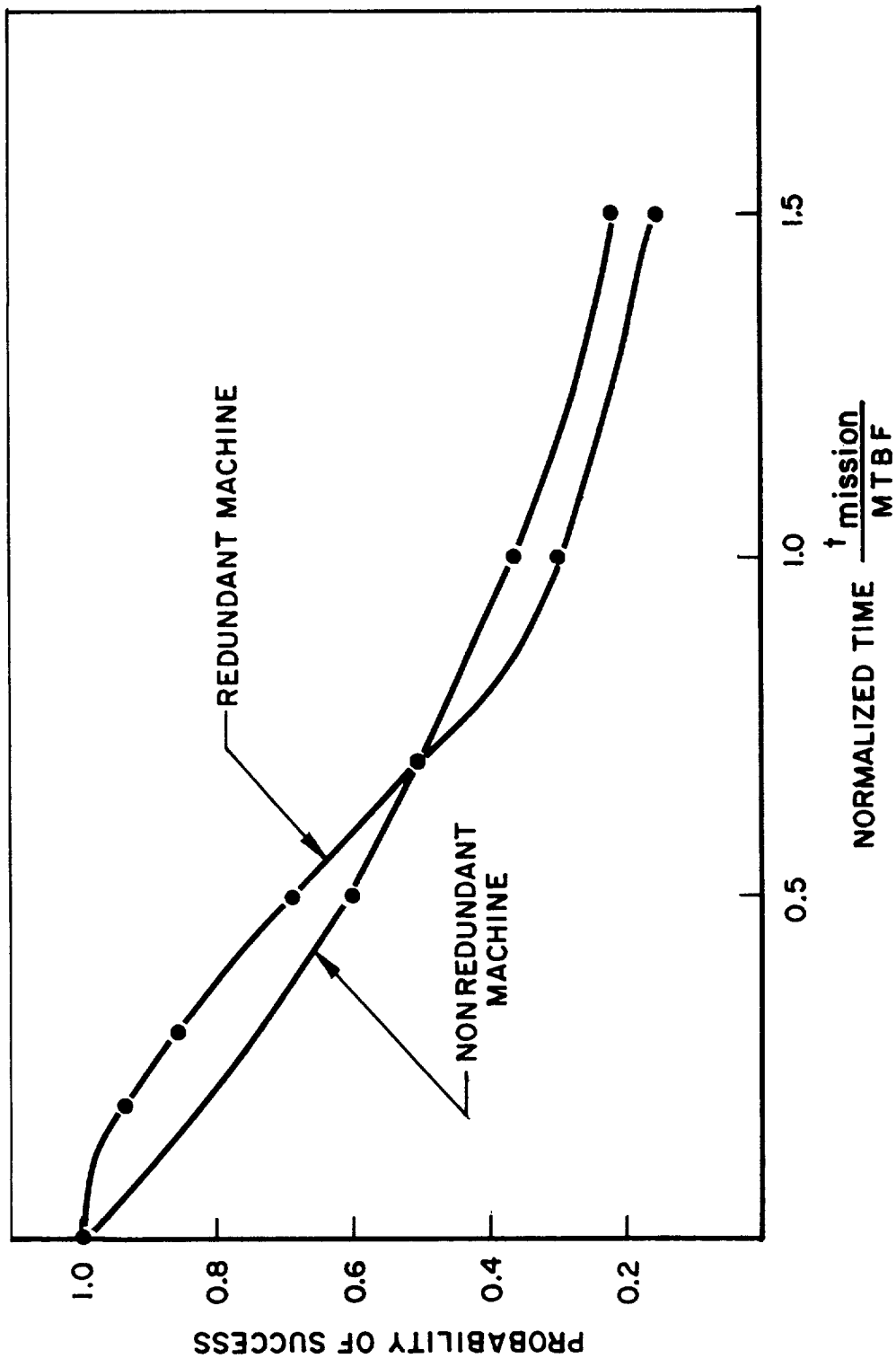


Fig. 8 Comparison of Non-redundant vs Redundant Computers

SECTION IV
INFLIGHT REPAIR

Since this computer has an inflight MTBF of 4000 hours, the probability of success is 0.966. Therefore, we must rely on inflight repair in order to realize the required probability of success of 0.99995. An inflight repair philosophy is contained in Appendix III. Recently more work has been done on techniques for inflight repair[1]. As a result of this investigation, we now have two approaches to accomplish inflight repair. The first of these approaches employs a device called the Micro Monitor which is designed to communicate with the computer when the malfunction makes the displays inoperative. The Micro Monitor plugs into the computer test connector at the front of one tray and makes it possible to force transfer of control directly to any desired memory location and read the contents of any location. The Micro Monitor is a scaled down version of the essential parts of the GSE equipment required for computer debugging. This device is known to be effective in direct proportion to the training and native skill of the operator and would enable a moderately skilled operator to isolate a large class of failures quite readily, down to three or less replaceable units. The disadvantages of this approach are that the Micro Monitor must be carried on board (the estimated weight is 5 to 10 lbs) and that the operator must exercise considerable thought as well as follow defined procedures to isolate a fault. An operator with training of three to six months should be able to locate faults and repair the computer within an hour.

The second approach is more systematic and by using it a single failure in a replaceable module can be repaired with certainty in about 1.5 hours. One half of all possible failures can be repaired in 20 minutes. In this approach, which is called the

"Systematic replacement" method, a spare module is assumed for every different kind of module (of the 29 spare modules). Using well defined procedures, the operator replaces certain groups of modules and then attempts to run a check problem using the display and keyboard. If the check can be accomplished the failure has been repaired; if not, another group of modules are replaced, etc. With the present mechanical design this replacement and check procedure will accomplish the repair with certainty in about 1.5 hours. The first step in the procedure, which takes about 10 minutes, has a probability of successful repair of 35%. The only aids required are the procedures on microfilm, the universal tool for extracting modules and one spare module for each different kind. Figure 9 is a curve of the probability of success as a function of time.

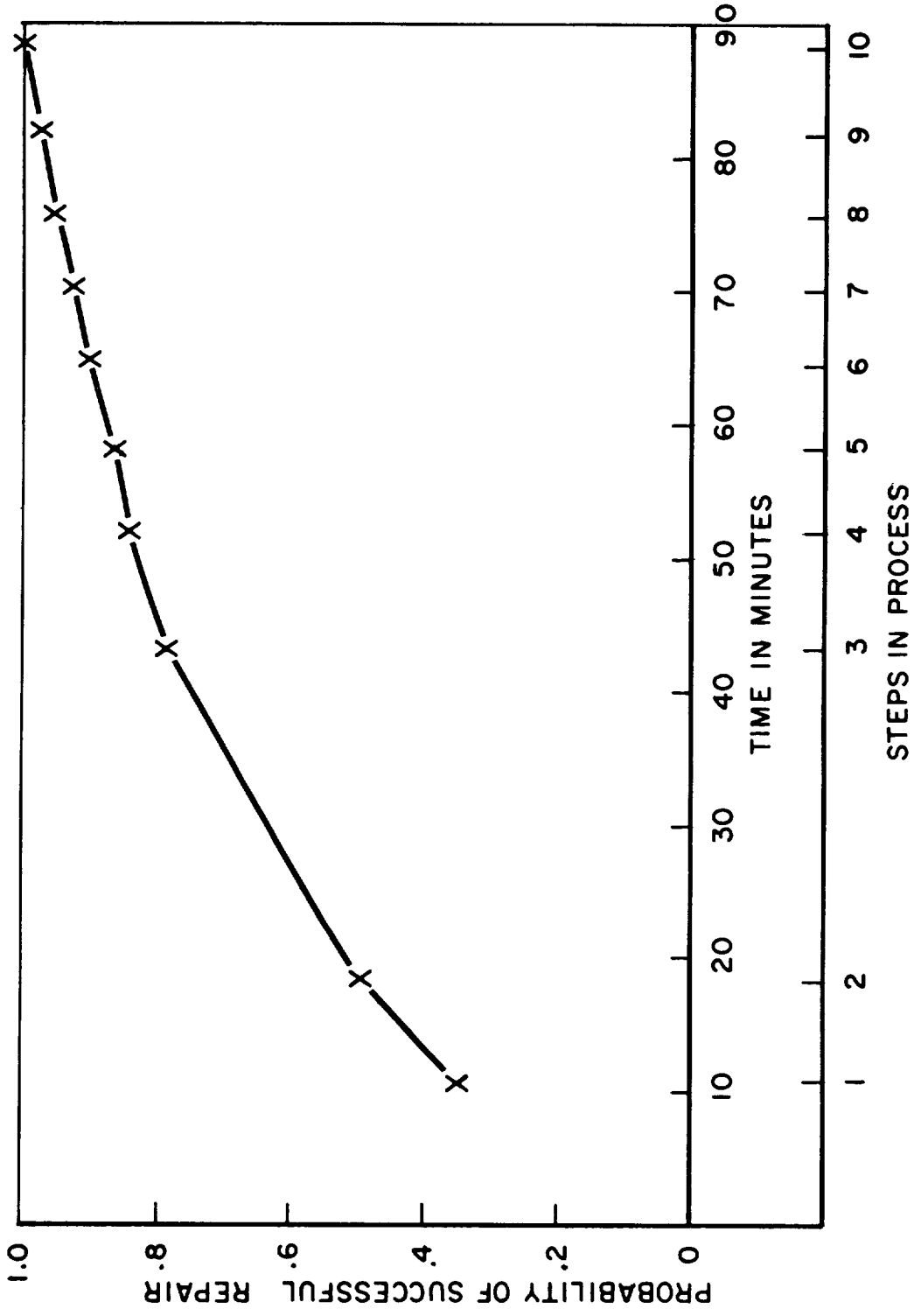


Fig. 9 Probability of Successful Repair

APPENDIX I

Using the LEM packaging form factors the computer will fit into the space allocated in the C/M (see Fig. 10 which is a photograph of this configuration in the mock-up of the C/M lower equipment bay). The two trays for logic and fixed memory are located in the center, the power supply and erasable memory tray on the lower right hand side with the G & N to C/M interface connectors directly above this tray. Note the power and servo assembly directly above the computer. Note also the space on the left of the computer for a complete tray of spare modules.

Fig. 11 is a side view of the computer tray assembly with both logic and rope memory modules shown plugged into the tray connector. The three modules labeled rope and the four labeled driver module is 6000 words of memory and its electronics. Four sections like this in the fixed memory tray will hold 24,000 words of memory and all the driver electronics. Four sections of the logic modules in the logic tray make up the complete logic section of the machine.

Fig. 12 is the power supply and erasable memory tray. One half of this tray contains the erasable memory and its electronics. The other half of the tray contains the power supply. In this LEM configuration this tray marries with one half of the fixed memory tray to become one of the two trays required for the LEM computer. Since fixed memory is now only one half a tray the memory capacity is reduced to 12,000 words.

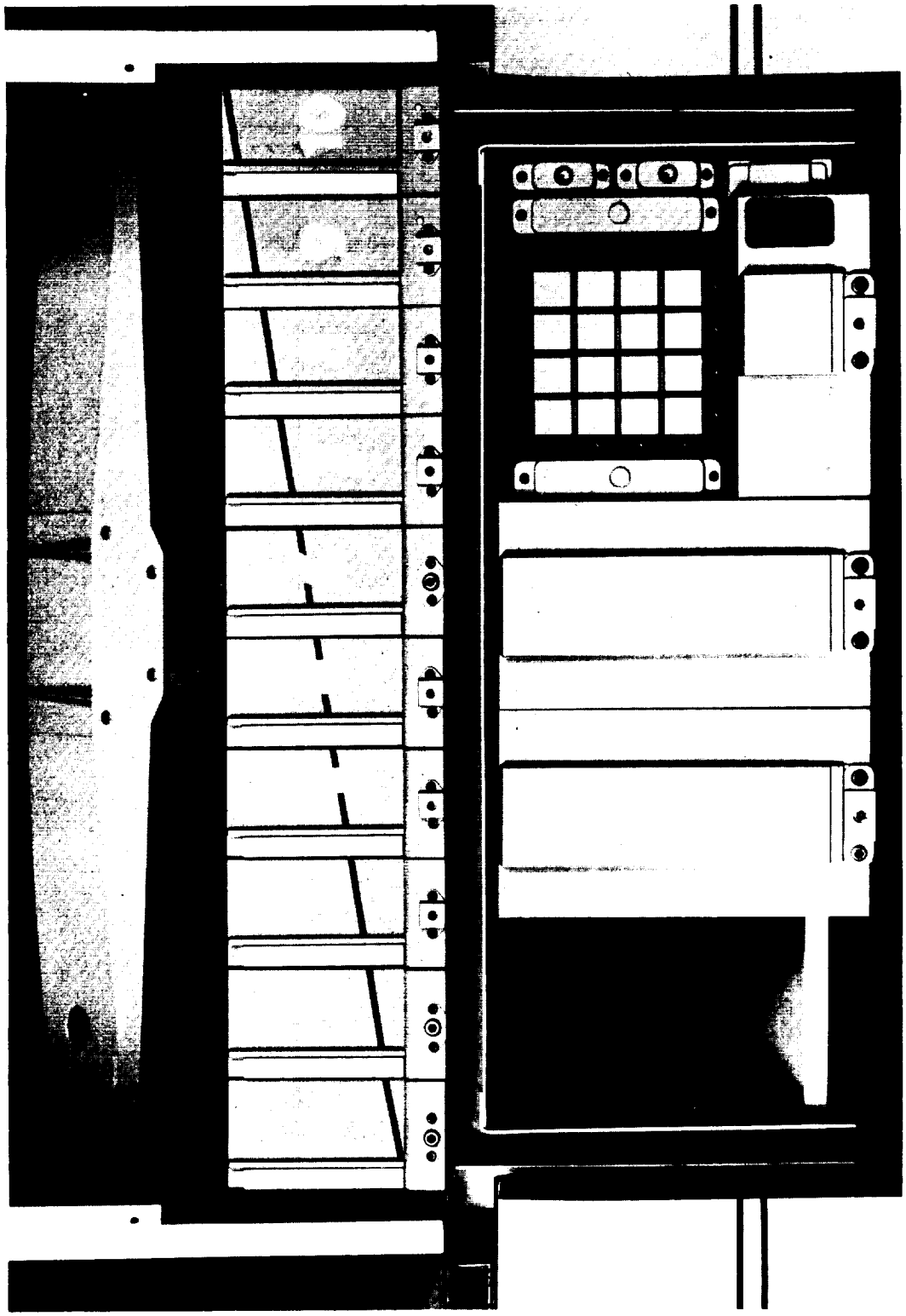


Fig. 10 Command Module Lower Equipment Bay

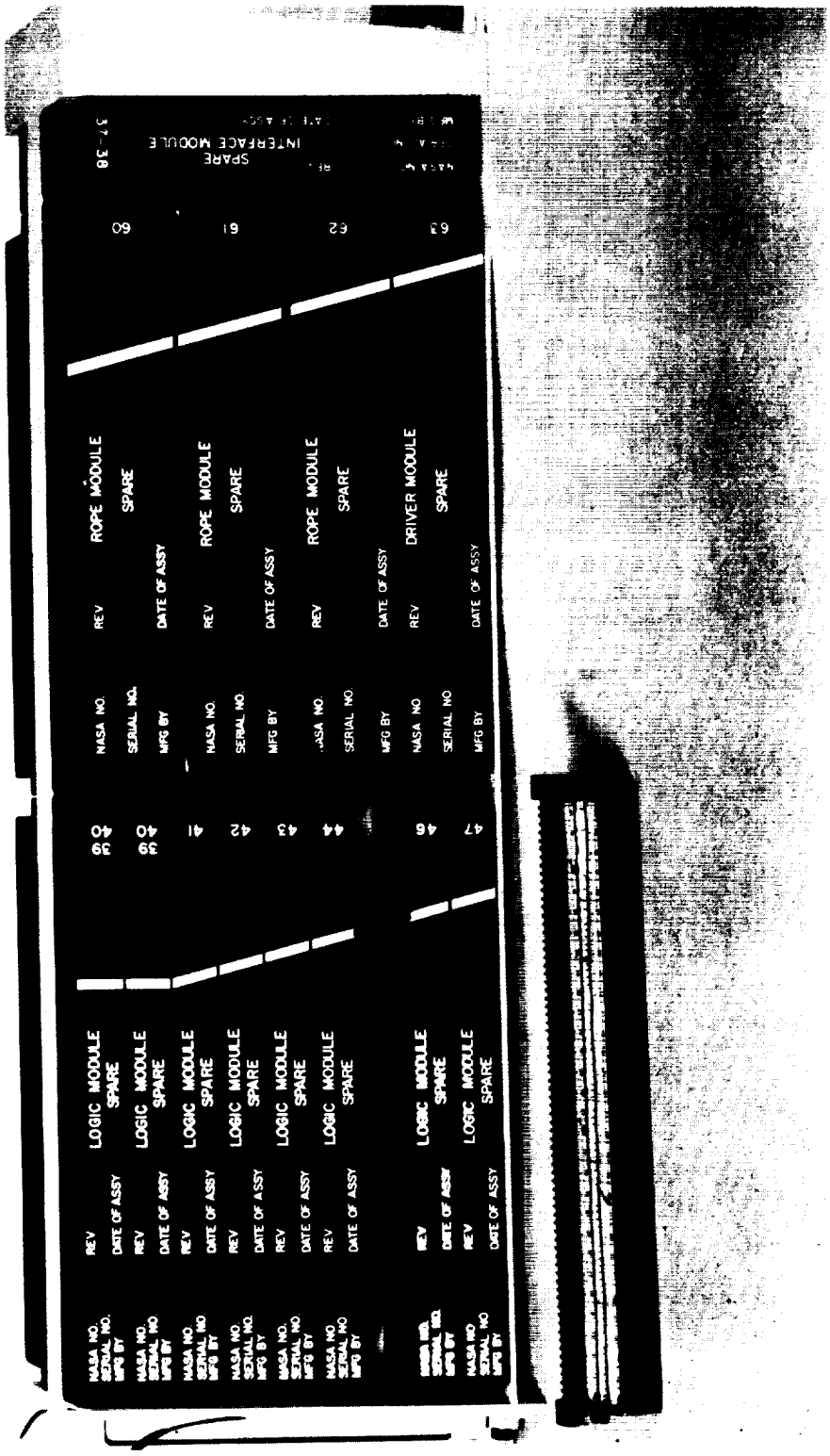


Fig. 11 Computer Tray Assembly

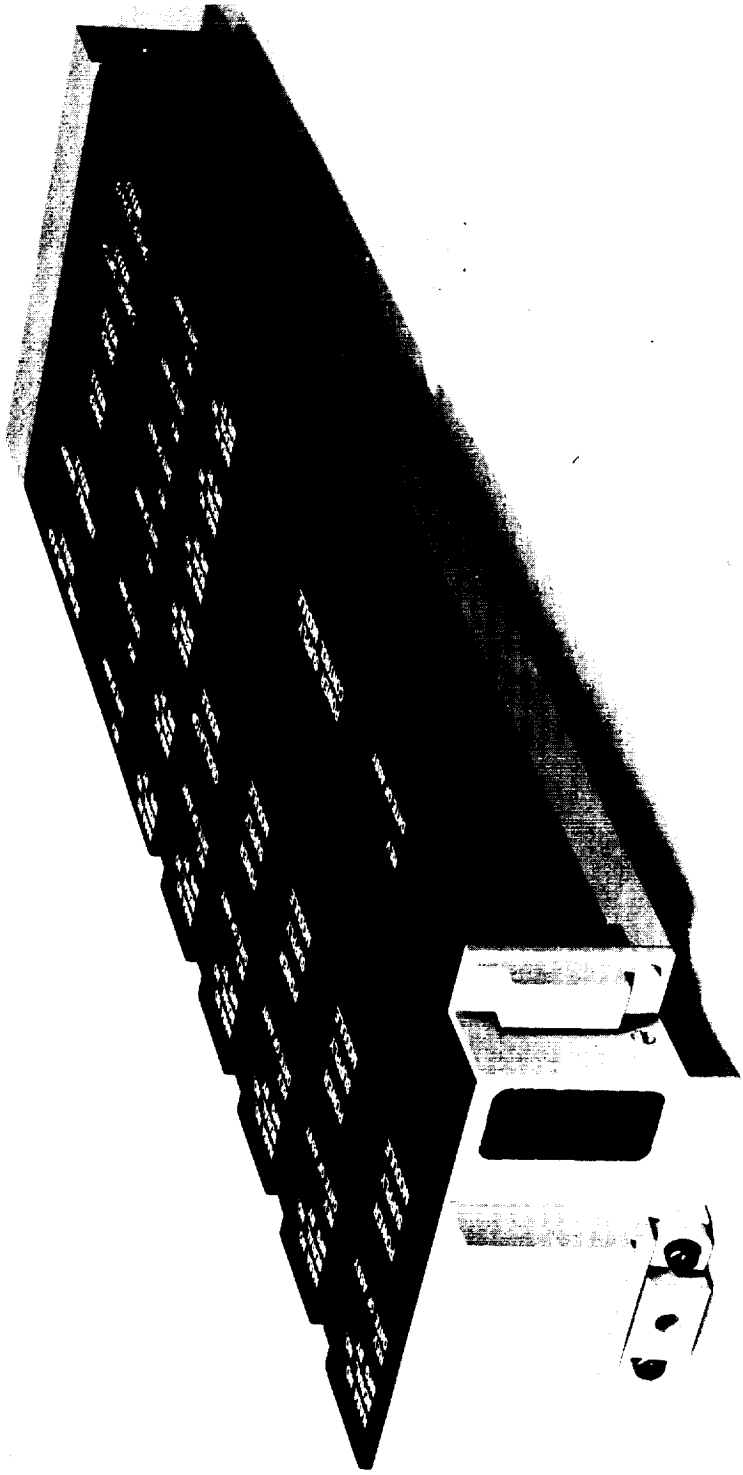


Fig. 12 Computer Power Supply Assembly

APPENDIX II

A. MEMORY AND LOGIC

The AGC uses three types of memory circuits. One is for permanent storage of instructions and constants, and holds about 24,000 words. A second type is for temporary storage of intermediate results, modified instructions, and input data. It holds about 1024 words. Both of these types of memory are relatively economical and dense in terms of number of words per unit volume, but they also require a comparatively long time to read from and write into (about 12 microseconds).

The third type of memory, consisting of sixteen registers, has a read-write time of about two microseconds, and is about 1000 times larger than sixteen words of the first two types of memory. This group contains the input and output registers, which communicate between the computer and the rest of the Apollo system, and the Central registers which participate in the steps within instructions that cause the desired mathematical transformations to be effected.

These three types of memory are employed to optimize the requirements for reliability and inflight maintenance without sacrificing the speed and flexibility requirements of the Apollo Guidance Computer. The permanent memory requires very few active components and very little power to operate. It also has properties that make it indestructible short of mechanical damage, that is, there is no inflight failure of any kind that can destroy this part of the memory. This property permits electronic failures to occur; these can be repaired, and the computer can be returned to full operation without extensive reprogramming and data entry. In this way, the permanent memory can be compared to a punched paper tape. The only way to destroy the information on the paper tape is to mechanically destroy the tape. The major disadvantage

of the permanent memory is that it takes time to make changes in the information stored since a new memory module must be built when a change is required. It is estimated that the time required to build the memory is less than two weeks and takes only a few minutes to install in the computer. The type of data stored in the permanent memory can be determined well in advance and any changes would require serious consideration and extensive studies before making changes. This disadvantage, the time lag of a few weeks for construction of the new memory, is not serious in the light of the inflight reliability advantages.

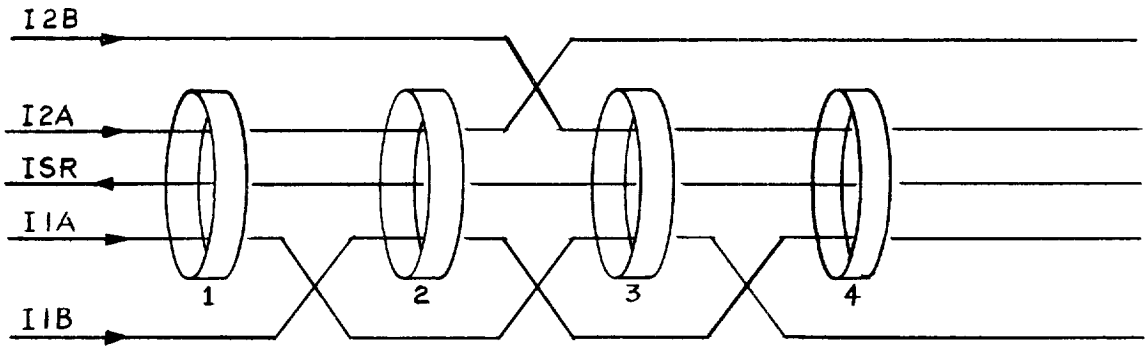
Data that must be changed during inflight computations or for last minute mission changes is stored in the second type of memory, the temporary storage. Data may be entered into this memory via any one of three methods:

1. the astronaut's keyboard,
2. the "PACE" digital command system before launch,
3. the up telemetry link during flight.

In case of inflight failure that destroys the information in this memory the computation can be restarted by reading in only a very few words.

The permanent memory employs a device called a Rope, which was developed at MIT/IL for a deep space probe computer. The Rope, so named for its physical resemblance to a rope, makes use of the non-linear magnetic properties of a ferromagnetic alloy called Permalloy. A group of 21 wires threading 1024 toroidal permalloy cores in a certain way can be made to carry currents such that any desired core will reverse the direction of its magnetization.

ROPE



4 Core Rope Selection (sense lines not shown)

The following is an example of the method used to switch the flux in one of the 1024 cores. Two pairs of inhibit wires and a set-reset wire are employed.

To switch core 1 apply I_{1B} and I_{2B} and I_{SR}

To switch core 2 apply I_{1A} and I_{2B} and I_{SR}

To switch core 3 apply I_{1B} and I_{2A} and I_{SR}

To switch core 4 apply I_{1A} and I_{2A} and I_{SR}

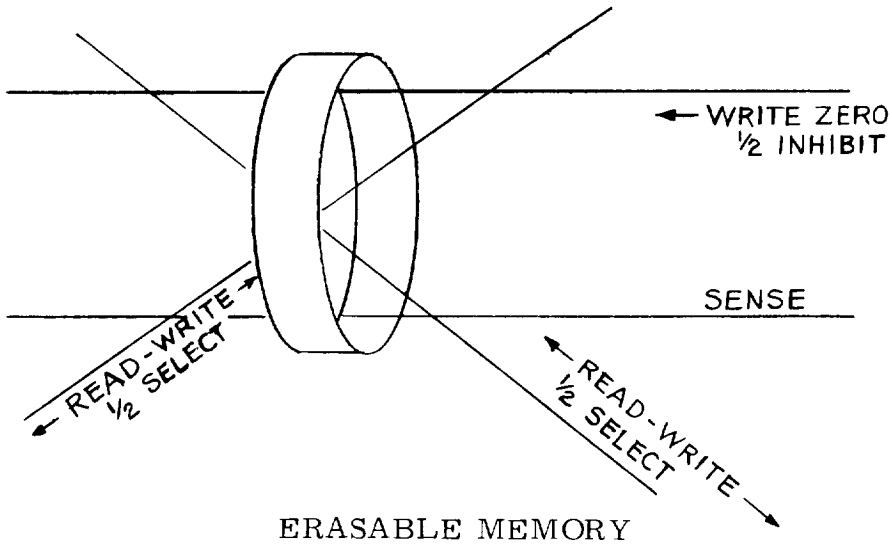
The inhibit currents prevent switching in the cores they thread. When one current of each pair is applied only one core is free to switch, and I_{SR} switches it. Afterwards, I_{SR} is reversed to restore the core to its initial state.

Ten pairs of inhibit currents select one of 1024 cores.

A switching core induces a detectable voltage between the ends of a sense wire which threads the core, but not in the wires which do not thread the core. The effect is the same as that in a

transformer, where a wire through a core is in effect a secondary winding with which one can sense changes in the core flux. A number of such wires, called sense lines, are threaded through the cores in the Rope. Thus a sense line will generate a binary one or zero for each core, depending on whether or not it threads the core. The number of sense lines in the AGC ropes is 64 and since the AGC word size is defined as 16 bits, it may be said that each core stores four 16 bit words. The address or location of a word is defined by the particular core which is switching, and by which of the four sets of 16 sense lines is being looked at. Ropes are wired-in storage; the information in them cannot be altered electrically.

The temporary or Erasable memory employs a large number of very small magnetic cores arranged in what is known as a coincident current array. Arrays similar to these are used in most computers made in recent years. The cores are ceramic instead of metal, but display nearly the same characteristics. Unlike the rope, the Erasable memory requires a separate core for each bit of a word since the value of a bit is determined by the direction of the last previous reversal of the core's magnetism as opposed to the geometric nature of storage in a rope (i.e., whether a wire threads a core or not).



ERASABLE MEMORY

The following is a brief description of the function of the erasable memory. One core, threaded by four wires stores a bit. Two wires select, one writes, and one senses.

The core is insensitive to current in a single select wire, but switches when there is current in both, unless there is current in the write inhibit wire at write time.

Information is represented by the direction of the core's magnetization, and is detected by trying to switch the core to the zero direction. If a voltage is induced at that time in the sense wire it means that the core was initially in the one direction.

To write into the core, the select currents are pulsed in the reverse direction. This will switch the core to a one unless inhibit current is simultaneously applied, in which case the core will remain at zero.

The Central registers are made of transistor circuits generally known as flip-flops. Each bit of storage requires two basic logical "building blocks", or NOR gates, for the flip-flop, plus two more to act as read and write gates.

The NOR gates used in the Central registers are used throughout the computer for various purposes, such as decoding of operation codes and addresses, generation of control signals, control of input signals, generation of output signals, and all of the other pulse forming and translating networks which are referred to as logic circuits, or just logic. The speed of a computer depends in part upon the transition times of the various logical elements used. In the AGC the NOR gate is the only type of logical element needed to make all of the necessary logic circuits, and its transition time is less than a tenth of a microsecond. This is fast enough for signals to propagate through various stages to develop the necessary results in the time alloted by the 12 microsecond memory cycle time.

B. INSTRUCTIONS

There are eleven instructions in the repertoire of the AGC. They were chosen from a wide variety of candidates on the basis of their usefulness in connection with the types of instruction sequences, or programs which were known to be desired for the Apollo mission, and for how expensive they would be to implement in terms of equipment.

The instruction set uses a central register called an accumulator, whose function is to store one of the operands for instructions involving two operands. It gets its name from the fact that the sum of two operands is placed there by an addition, so that the sum of several numbers can be accumulated by a series of additions.

The instructions include the four basic arithmetic operations of Addition, Subtraction, Multiplication, and Division, and one logical operation, Mask, which forms a word composed of the bit by bit logical products of the two operand words.

There are three data handling instructions for the transfer of numbers between the memory and the accumulator. One transfers from the accumulator to memory. One transfers the negative of the number in memory to the accumulator. The other exchanges the contents of accumulator and memory.

There are two sequence-breaking instructions. One specifies an address at which to begin a new sequence of instructions. The other causes the computer to skip one or more instructions if the operand is of a particular sign and magnitude.

One instruction is used to modify the instruction which follows it by adding to it the contents of a specified memory register.

C. INCREMENTS AND INTERRUPTS

The AGC includes some non-voluntary instructions which

set it apart from a typical general purpose computer. They are frequently found in computers required to operate within time-dependent systems. These instructions are not under the control of the instruction sequence. They are executed when certain signals from outside the computer cause the computer to interject them at a convenient point.

There are two types of non-voluntary instructions in AGC. One causes a register in erasable memory to be altered, either by adding one, subtracting one, or doubling. There are twenty registers which can be so treated, and forty separate input signals which can cause them to be so treated. The primary use of these registers, called counters, is in analog to digital conversion, i.e., reading the status of electromechanical measuring instruments to high precision. Pulses which indicate changes in the positions of instrument armatures are accumulated in their respective counters as they occur, without the need of scanning by elaborate programs. Other counters are used to keep a record of time, to keep track of output pulses from the AGC to other subsystems, and to receive information from the ground control center via the up telemetry link or the PACE command system.

The second type of involuntary instruction is the program interrupt. Events which require special immediate attention can cause the computer to transfer control to a sequence designed to cope with the event. A subsequent resume operation returns the computer to the original program at the point at which it was interrupted. Six different events are so treated: certain system error signals, keyboard entries, preselected time markers, display time markers, up link word completion, and certain armature zero signals. Both increments and interrupts will occur as a matter of course, and do not imply system abnormality when they occur. The speed with which the computer can execute a sequence of ordinary instructions is reduced as the activity of increments and interrupts increases. The execution time of an

increment is about 12 microseconds. If increment requests arrive at a total rate of 85,000 per second, ordinary instruction execution is virtually stopped, since increment requests take precedence over instructions.

D. INPUT AND OUTPUT

The AGC supplies pulses at controlled rates and in controlled numbers to the electromechanical components of the guidance system in order to orient, scale, and otherwise operate them. The pulses originate in a circuit called a scaler which generates pulsed wave forms of 0.78125, 1.5625, 3.125, 6.25. 12.5, 25, 50, 100, 200, 400, 800, etc., up to 102,400 pulses per second. These pulses are routed to various destinations by output registers which are similar to the central registers in that they are made of flip-flops. The various bits of the words stored in the output registers control the various pulse outputs. Some output bits have functions other than pulse rate generation. Some control the numerical computer displays to the crew of the spacecraft. Others are sent to the telemetry interface circuit to be transmitted to the ground control center. Others provide commands to other spacecraft systems.

The inputs to the computer are of two classes. One is the class of pulse inputs to the counter increment circuit and the program interrupt circuit. The other is the class of pulse or D.C. inputs to the input registers, where composites of input bits may be processed like other computer words.

APPENDIX III

AG 167-63
15 March 1963

NASA
Manned Spacecraft Center
Houston 1, Texas

Attn: Mr. Dave Gilbert

Subj: Inflight Testing & Maintenance

Gentlemen:

In the meetings on Feb. 27 and 28, 1963, with various representatives of NASA, the ground rules for inflight testing were defined. NASA requested information on the test philosophy for the AGC. The following is the first cut at a definition of this AGC inflight test philosophy.

Ground Rules & Requirements

These are copied from the minutes of the MIT/MSC Pace Meetings of Feb. 27, 28.

1. There will be a meter in the IFTS.

2. There will be a scanning comparator in the IFTS.

3. No oscilloscope, but may add one if a requirement is shown.

4. There may be a movable probe (presumably connected to the meter).

5. The astronaut and the vehicle may be used for fault isolation.

6. Only replaceable modules will be checked.

7. Sufficient access points are required to isolate faults to within 3 or 4 modules.

An additional assumption is that only single failures will be considered.

Requirements on IFTS

MIT requires that the following points be connected to the inflight test system for test and maintenance of the AGC subsystem.

1. Temperature

2. Power monitoring points
   GND
   +3V(A)
   +3V(B)
   +13V

3. Lowest frequency scaler signal (1.25 cps square wave) for observation of the oscillation on the meter.

There are no further requirements on the IFTS for the reasons listed below:

a. The AGC has self testing capability.

b. The testing equipment provided (i.e., the meter) is inadequate for examining signals with rise times of the order of .1 msec.

c. Even assuming a 'scope, it is doubtful that it could be of much help because there are very few computer points at which a stationary pattern may be expected.

d. The loading due to the capacity in the cabling to the IFTS would, in most cases, prevent proper functioning of the computer. It would be necessary to provide buffering circuits.

e. Excessive cabling would be required between the IFTS and the AGC.

Fault Detection

To meet the requirements for inflight maintenance, the AGC will rely heavily on self testing programs and on various error detecting circuits designed into the computer. The circuits and displays provided are capable of detecting faults and can be used to isolate these faults to repairable sub-assemblies.

During normal operating modes of the G&N System, the signals sent to IFTS, the G&N alarm indicators and the function of the computer display and controls will be capable of detecting at least 90% of all possible failures in the computer sub-assembly. Abnormal behavior of other G&N sub-systems and computer self test routines will detect the remaining 10% of the failures. There

may be a very small percentage of faults which will require comparison with ground tracking data in order to detect the fault.

During checkout modes of operation, the computer self test routines will be capable of detecting 98% of all faults in the G&N. Exercising the G&N or the S/C can detect the remaining faults.

Fault Location

To accomplish fault location, it is assumed that all computer inputs and outputs can be decoupled from the other subsystems. The one exception to this is the clock synch to the S/C central timing system. It will not be interrupted unless there is a failure in the clock. It is also assumed that step-by-step instructions will be available for the astronaut. Briefly these instructions are as follows:

1. For faults in the displays: Displays are redundant, operating in parallel; therefore they may be used to check each other by comparison tests.

2. For faults internal to AGC: A series of subroutines is initialed through the keyboard by the astronaut. These routines will check that all the instructions are properly executed and that both memory and arithmetic units are operating correctly. The likelihood of these tests being completed successfully if there are malfunctions in memory control or arithmetic units is extremely small. These routines are not "debugging" or maintenance routines; they are intended for rapid checking of the correctness of the AGC.

3. For faults in the input/output of the computer: Another set of subroutines are used with the AGC disconnected from the G&N and S/C. Here a self test plug is used to connect computer output into computer inputs. The routines called for in this case check that all interfaces are there and that they are electrically sound.

   These routines and procedures will isolate faults in the G&N System to within or without the AGC. If the fault is within the AGC, it may be isolated to less than 5 replaceable sub-assemblies.

Maintenance

In general, the maintenance procedure consists of matching the symptoms exhibited by the AGC (the alarms in particular) with check lists available for the astronaut. These lists will have

indications of probable causes of the failure and operation instructions for further tests or an indication of stick at fault.

To accomplish the repair it is assumed for the purpose of this report that there are 100% spares. With this assumption better than 98% of the faults can be located to one stick by replacing one of the 3 to 5 sticks suspected of faults then repeating the self tests described, etc. until the faulty stick is removed. The tools required to remove sticks is assumed to be part of S/C supplies.

Very truly yours,

Eldon C. Hall
Division Director
Computer Development

ECH:ms

Dist.

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